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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/849,126	05/04/2001	Avraham Mualem	042390.P10990	9064

7590 06/09/2005

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EXAMINER	
DINH, MINH	

ART UNIT	PAPER NUMBER
2132	

DATE MAILED: 06/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/849,126	MUALEM ET AL.	
	Examiner	Art Unit	
	Minh Dinh	2132	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This action is in response to the amendment filed 03/23/2005. Claims 1-23 have been cancelled; claims 24-43 have been added.

Response to Arguments

2. Applicant's arguments filed 03/23/2005 have been fully considered but they are not persuasive.

Applicant argues that Anand (6,370,599) teaches offloading processing tasks from the computer system to the NIC and therefore, Anand teaches away from the computer system generating a security association (SA) (p. 7, 1st paragraph). Anand teaches offloading IP security functions from the CPU of a computer to a NIC; however, the specific SA information for performing an IP security function is generated by the CPU and transferred to the NIC (col. 10, line 64 – col. 11, line 6).

Anand does not teach data verification between the computer (i.e., the CPU) and the NIC, which is a peripheral device. Yoshida (5,928,372) teaches data verification in a data transfer system in which a host processor transfers data and an associated integrity indicator to a peripheral device (i.e., the hard disk unit) and the peripheral device verifies the integrity of the data and provides the verification result to the host processor (col. 1, line 60 – col. 2, line 20; figures 20-21). Applicant argues that Yoshida is directed to method and apparatus for verifying data transferred between a data processor and an external recording unit (p. 7, 2nd paragraph). Yoshida's external

recording unit, the hard disk, is a peripheral device and that Yoshida and Anand are analogous art because they are from a similar problem solving area, which is transferring data from a host processor to a peripheral device.

Claim Objections

3. Claim 39 is objected to because of the following informalities: the phrase "at least one network adapter being capable of being coupled to an information handling apparatus" (line 1) and "is substantially similar the SA generated" (line 7). They are interpreted respectively as "at least one network adapter being coupled to an information handling apparatus" and "is substantially similar to the SA generated". Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 25-26, 30-31, 35-36 and 40-41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Each claim recites the limitation "and has computations" at the end. The limitation is supposed to be the last method in a list of methods for generating an integrity indicator. It is not clear what the limitation means. The claims are examined based on other listed methods.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 24-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anand et al (6,370,599) in view of Yoshida (5,928,372).

Regarding claim 39, which are representative of claims 24, 29 and 34, Anand discloses a system comprising: a network adapter being capable of being coupled to an information handling apparatus (IHA) via a bus (fig. 1, elements 53, 21-23), said network adapter comprising an integrated circuit capable of receiving a security association (SA) generated by said IHA (col. 8, lines 21-35; figures 3-4 and corresponding text). Anand teaches transferring data from the IHA (i.e., the CPU) to the network adapter; however Anand does not teach verification of data transferred between the CPU and the network adapter, which is a peripheral device. Yoshida teaches data verification in a data transfer system in which a host processor transfers data and a first integrity indicator generated by the host processor to a peripheral device (i.e., the hard disk unit) and the peripheral device generates a second integrity indicator, verifies that the received data is similar to the data sent by the host processor by comparing said first integrity indicator to said second integrity indicator (col. 1, line 60 – col. 2, line 20; figures 20-21 and corresponding text). Anand and Yoshida are

analogous art because they are from a similar problem solving area, which is transferring data from a host processor to a peripheral device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Yoshida's teaching of data verification into the Anand system in order to insure the correctness of the reception data (col. 9, lines 47-54). Accordingly, the IHA generates and sends a first integrity indicator to the integrated circuit, the integrated circuit receives the first integrity indicator, generates a second integrity indicator based on said SA, verifies that said SA received by said integrated circuit is substantially similar to the SA generated by said IHA by comparing said first integrity indicator to said second integrity.

Regarding claims 25-26, 30-31, 35-36 and 40-41, Yoshida further discloses that the data checking integrity method used to generate the first and second integrity indicators is a cyclical redundancy checking computation method, a checksum computation method or a parity checking method (col. 10, lines 55-67).

Regarding claims 27, 32, 37 and 42, Yoshida further discloses that the peripheral device indicates the integrity of the data received to the host processor (figure 21, element 24).

Regarding claims 28, 33, 38 and 43, Yoshida does not explicitly disclose setting an integrity error indicator bit in a memory of the host processor. However, this feature is deemed to be inherent to the Yoshida method as element 24 of figure 21 shows that the peripheral device provides the comparison result signal to the host processor. The

Yoshida method would be inoperative if there were no register/memory on the host processor to store the comparison result signal.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Dinh whose telephone number is 571-272-3802. The examiner can normally be reached on Mon-Fri: 10:00am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on 571-272-3799. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MD

Minh Dinh
Examiner
Art Unit 2132

MD
6/1/05

GILBERTO BARRÓN JR.
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